Jamieson T. Olsen

Engineering Note

Date: 6 January 2003
Rev Date: 18 February 2003

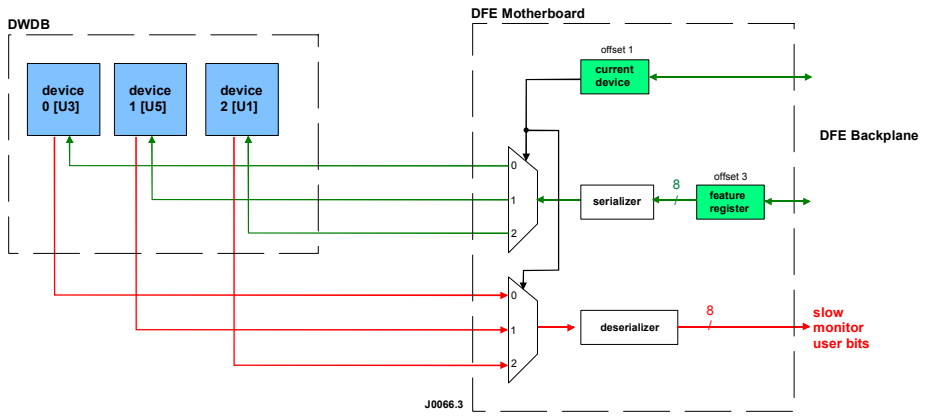
Project: L1CTT / CTOC
Doc. No: 2003-01-06a

Subject: L1 CTOC Control and Status Specification

Introduction

The L1 CTOC firmware resides in device 2 (U1) of the CTOC "Double Wide" daughterboard. This document describes how to set post-initialization variables and control what status information is passed back to the slow monitor system.

A New DFE Motherboard – DWDB Interface

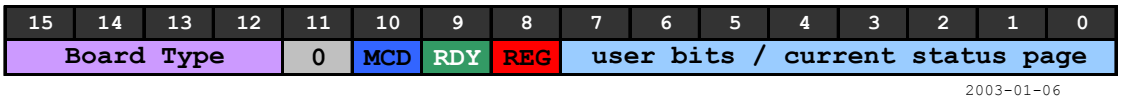


This new interface replaces the FIRMWARE REVISION REGISTER logic. A new register called the feature register is located at **base_addr + 3** on the DFE backplane. This register is readable and writeable from the DFE backplane. When written, the contents of the register are automatically serialized and sent to the current device. (Unlike the older design, a board reset is not needed to initiate this transfer.)

Each DWDB device constantly serializes 8-bits of status information and sends that down to the DFE motherboard. Depending on the value of the current device register, one of the three devices is selected and that data is de-serialized and becomes the slow monitor user bits[7..0].

For this interface to work the DFE Motherboard must have U49 firmware **1.42** or newer. Also this circuitry will not function unless all devices on the DWDB are initialized (ready bit set). In order for a DWDB device to accept bytes from the feature register and also serialize the 8-bits of status information, it must instantiate a module called *mobo_int.vhd* at its top level.

New Slow Monitor Status Word



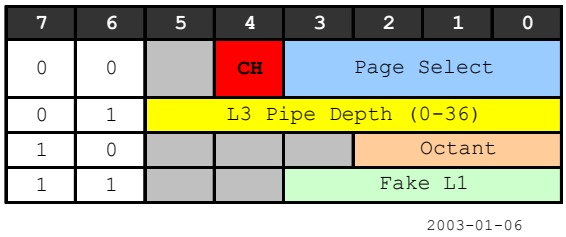
DFE Motherboard firmware v1.42 changes the meaning of the slow monitor status word. The master clock detect (MCD) has been moved from bit 0 to bit 10. RDY is set when all of the devices on the CTOC board have been initialized. REG is **cleared** if there is a problem with one or more of the voltage regulators in the DWDB. Bits 7..0 are available for the user bits. The board type for CTOC is 0001.

Setting Post-Initialization Variables

After the L1 CTOC device is initialized with production firmware, some additional arguments must be passed to it. These are:

- **L3 Pipeline Depth**. This is adjustable from 0-36 crossings deep. The default is 33.
- **Home Octant**. The firmware needs to know what its home octant is. Range is 0-7, default is 0.
- **Fake L1 record select bits**. For diagnostic purposes, the L1 CTOC can send fake L1 records to the CTTT. Default is zero.
- **Status Page**. The L1 CTOC has a lot of status information, but it can only be viewed in one byte-wide "page" at a time. Default is page 0.

As previously mentioned, the new DFEM-DWDB interface supports writing and reading an 8-bit value to/from each device on the DWDB. This is does not provide enough bits to do everything the L1CTOC needs it to do, so a simple protocol is imposed on this interface. The feature register now has four independent registers, selected by bits 7 and 6:



So to change the L3 Pipeline depth to 25 do the following:

```
set DFE 3
set device 2
# 25 = 0x19.  Now OR 0x19 with 0x40 to set bit 6.
cmd writebyte 3 0x59
```

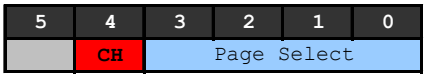
And to change the Octant to 5 do the following:

```
set DFE 3
set device 2
# 5 = 0x05.  Now OR 0x05 with 0x80 to set bit 7.
cmd writebyte 3 0x95
```

Selecting Status Pages

The L1CTOC supports 16 pages of status information. Each page is a single byte of status information. The current status page becomes the slow monitor user bits for the CTOC board. Previous versions of the status information used logic to stretch error pulses so that spurious errors had a better chance of being sampled by the slow monitor system. However, this method had shortcomings and has been replaced with a status "history" scheme.

Status history works like this: after reset all of the L1CTOC status pages are set to 0x00. On every 53MHz clock edge the contents of the status pages are updated. If a bit goes high, it stays high until the status page history is cleared. Setting Bit 4 of the Page Register clears the status history for the status pages.



- ***After power up or board reset the history bits may contain garbage. So it is good practice to clear the history after these conditions.***
- ***The history is cleared on the 0 to 1 transition of the CH bit. When clearing the history it's best to explicitly toggle it by writing 0x00, 0x10, and 0x00.***

Below are the 16 status pages specific to the L1CTOC design.

page	S7	S6	S5	S4	S3	S2	S1	S0
0		Bad Master FX	FX XOR	L2	Parity Err	Missing Link	Sync Err	Tick/Turn Locked
1						Home Octant Number [2..0]		
2					Fake L1 Mode			
3			L3 Pipeline Depth [5..0]					
4								
5	0	1	0	1	0	1	0	1
6	1	0	1	0	1	0	1	0
7								
8				Miss-link4	Miss-link3	Miss-link2	Miss-link1	Miss-link0
9				Miss-link9	Miss-link8	Miss-link7	Miss-link6	Miss-link5
10				Sync-err4	Sync-err3	Sync-err2	Sync-err1	Sync-err0
11				Serr-err9	Sync-err8	Sync-err7	Sync-err6	Sync-err5
12				Parity-err4	Parity-err3	Parity-err2	Parity-err1	Parity-err0
13				Parity-err9	Parity-err8	Parity-err7	Parity-err6	Parity-err5
14				Patt-err4	Patt-err3	Patt-err2	Patt-err1	Patt-err0
15				Patt-err9	Patt-err8	Patt-err7	Patt-err6	Patt-err5

2003-01-06

NOTE: the orange cells are cleared by the clear history feature.

Parity Err. logical OR of the ten Parity Error bits in pages 12 and 13.

Missing Link: logical OR of the ten Missing Link bits in pages 8 and 9.

Sync Err. logical OR of the ten SYNC_ERR bits in pages 10 and 11.

L2. Set when a L2 record comes into the L1CTOC on link2.

Tick/Turn Locked. The L1CTOC extracts two trigger framework bits (First Crossing, CFT_RESET) from the DFEA L1 records delivered on link 2. From these control bits the L1CTOC determines the beam timing and maintains a tick and turn counter. If this LOCKED bit is set it means that the L1CTOC has observed a CFT_RESET followed by an FX and it is incrementing the tick and turn counters normally. Tick and Turn counts are only used for L3 readout – they do not affect the L1 output of the CTOC in any way.

Bad Master FX: Once the tick and turn counters are locked they expect the FX bit to come in at a specific time. If FX comes in at another time this bit is set, and it stays set until the history is cleared.

FX XOR: Every time a L1 record comes into the L1CTOC all of the FX bits are compared against the master FX bit extracted from link2. This bit is the logical XOR of the individual FX bits— if the FX bits disagree, this bit is set and stays set until the history is cleared.

Status Pages 1-3 always returns the value of their associated registers.

Status Pages 5-6. 0x55 and 0xAA, respectively. Used for debugging the interface.

Status Pages 8 and 9. The Missing Link error bit for each input link is listed here. If a link has not seen a Beginning of Record (BOR) transition in at the last 63 clock cycles, the corresponding bit is set and stays set until the history is cleared.

Status Pages 10, 11. After the links have been synchronized, a circuit checks that each link's BOR signal is aligned with the master BOR signal. If there is a synchronization problem with a link, the corresponding bit is set and stays set until the history is cleared. Only considers non-missing input links.

Status Pages 12 and 13. As L1 records come into the L1CTOC, the horizontal parity bits are checked for frames 1-6. If there is a parity error in the first 6 frames of the L1 record then the corresponding bit will be set and stays set until the history is cleared. Only considers non-missing input links.

Status Pages 14 and 15. The L1CTOC contains test record detection circuitry. The DFEA can be placed into a special mode where it sends a L1 test record to the L1CTOC. *Used only for DFEA to L1CTOC LVDS link tests.*

Some Examples:

To change the L3 pipeline depth to 30 and confirm it:

```
set DFE 3
set device 2
# change the L3 pipe depth to 30. (0x1E || 0x40 = 0x5E)
cmd writebyte 3 0x5E
# now set the current page to 3
cmd writebyte 3 0x03
# now the user bits = status page 3
get userbits 3
# user bits should equal 0x1E
```

To clear the history and then rapidly collect all of the status pages:

```
set DFE 3
set device 2

# clear history and set current page to 0
cmd writebyte 3 0x00
cmd writebyte 3 0x10
cmd writebyte 3 0x00
# read status page 0
get userbits 3

cmd writebyte 3 0x01
get userbits 3

cmd writebyte 3 0x02
get userbits 3

cmd writebyte 3 0x03
get userbits 3

....
```